

Reduced Stresses Inside Semiconductor Chips Lead to Higher Reliability

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Semiconductor manufacturers, thanks to technological advances that are leading to a continuous scaling of lithographic dimensions, are creating integrated circuits (ICs) that are increasingly smaller. Reducing silicon consumption without decreasing device reliability can mean multiple millions of dollars in cost savings. Thus, Pad Over Active (POA) structures have been implemented in most advanced semiconductor technologies in order to optimize area consumption. With it, active circuitry is designed below test/bonding pads to exploit the interconnection properties of multilayer metal stacks. Simulation with COMSOL Multiphysics® allows STMicroelectronics to study these effects and formulate design rules that lead to robust circuits.

Multilevel Interconnections

In an IC, it's necessary to carry signals from one subcircuit to another, and for this purpose a chip uses multiple layers of metal interconnects, each separated by an interlevel dielectric (ILD) layer. Small conductive plugs called vias, often made of tungsten, pass signals from the silicon to a metal layer and also from lower metal layers to the upper one (Figure 1). Further, an IC needs conductive pads on the surface that connect to internal circuitry for two reasons: first, to serve during final

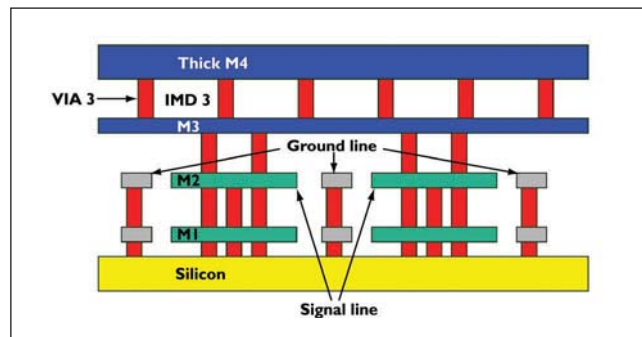


Figure 1: In an IC, circuitry on the silicon layer is connected through metal signal traces (horizontal connects), which in turn are connected to the silicon layer and other metal layers with solid tungsten plugs called vias (vertical connects).

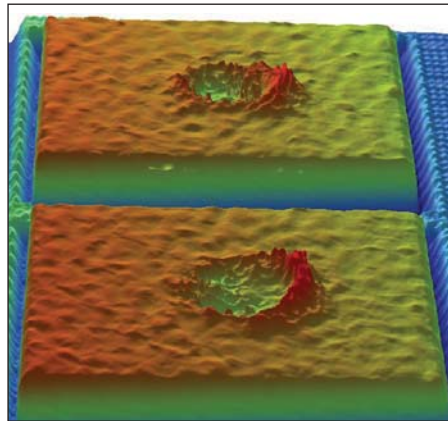


Figure 2: When a probe tip drops down onto a pad with excess force, it creates an uneven surface that can make soldering a bonding pad more difficult.

manufacturing as spots for the attachment of bondouts, which carry signals from the IC itself to the pins of the final package in which it is mounted and then shipped; second to serve as test points to verify that a device is working properly in what is known as electrical wafer sort (EWS).

EWS is conducted on each IC so as to evaluate its functionality before assembling it in a package and installing it in a final application. This testing is performed by making contact with a pad using a suitable probe by lifting the wafer (which is mounted on a chuck) until contact is established with needles that are inserted in a dedicated card; this condition is considered the reference status (zero level). For Smart Power ICs, due to both the high current levels required and the presence of very precise analog stages, good electrical contact between the needle tip and the pad surface is mandatory. For this reason, an additional overdrive must be applied to the chuck. At the same time, the pressure of the

tip on the pad surface must be limited so it does not induce cracks in the ILD layers. Metal extrusion inside of these cracks can, in fact, lead to electrical failures. It is therefore appropriate to investigate and simulate the process so as to reduce the number of experiments, save time and money, and improve the probe's design.

Probe Design Optimization

One of the most important targets for the EWS process is to limit the induced damage on a restricted surface. The probe tip can scrape the pad surface and create an unevenly shaped crater (Figure 2), and such a wide damaged area does not allow for a reliable bonding process.

To investigate in detail what happens when a probe tip hits a pad surface, the team at STMicroelectronics decided to use COMSOL Multiphysics in cooperation with one of its probe suppliers (Technoprobe, Italy). The team was made up of people involved in Technology CAD, POA structures development and EWS testing inside STMicroelectronics as well as people dealing with the development of probe cards at Technoprobe. The goals were to:

- 1) validate a COMSOL model with measured data
- 2) optimize the probe's design to increase the performance of the EWS process.

To get the project started, Technoprobe provided STMicroelectronics with

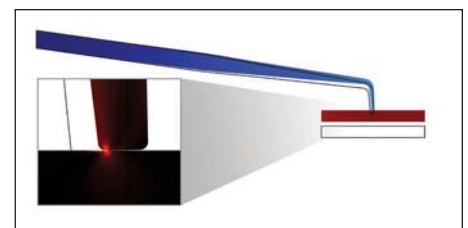


Figure 3: The top plot shows the displacements in the probe and the pad; the white shows the initial contact position and the colored plot its final position when the chuck is raised up. The zoomed area shows a plot of the von Mises stresses in the contact area that need to be investigated carefully in order to limit the induced damage.

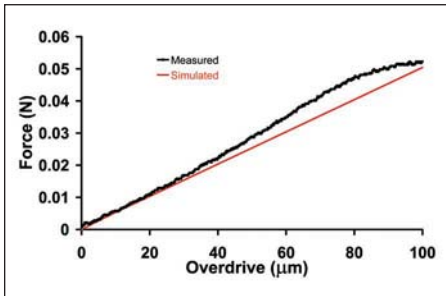


Figure 4: Simulated vertical contact forces versus the applied overdrive compared to the measured forces. The reference position is when the pad first comes in contact with the probe (zero level).

a CAD drawing of the current design of the probe as well as material data. Then, with the help of the Structural Mechanics Module, STMicroelectronics was soon able to develop a 2D mechanical contact model (Figure 3). The results were then compared to measured data (Figure 4).

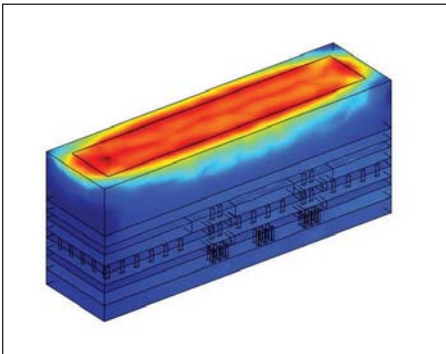


Figure 5: 3D geometry of an IC subsection used as the basis of a COMSOL model to measure stress in the ILD layers. Shown are the von Mises stresses.

“It was only with the COMSOL® model that we could determine the areas of peak stress and understand how failures could arise.”

Because comparisons with the results from the model were satisfactory, the team decided to continue to model in 2D and optimize the probe’s design.

The optimization of the probe’s geometry resulted not only in a new and thinner body but also a longer tip. The modified design resulted in better contact between the tip and the pad, less contact force and a shorter probe mark length. The model and later experiments confirmed that the

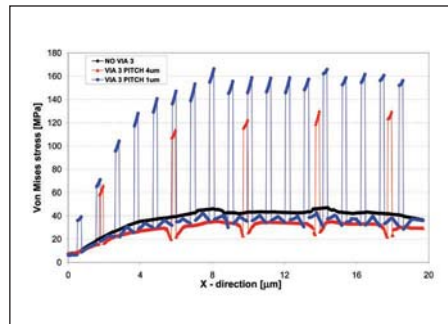


Figure 6: Von Mises stress in a semiconductor chip inter layer dielectric as a function of via pitch.



Figure 7: Authors Luca Cecchetto (left) and Lucia Zullino examine a model of the IC probe.

new configuration provides the equivalent electrical performance with 30% less force.

Modeling the ILDs

To improve the pad’s mechanical robustness, a 3D model (Figure 5) of the pad structure and the ILD layout was simulated. Figure 6 plots the von Mises stress in the top ILD for several via pitches. The black line shows the stress without vias, and there are no stress peaks. The other curves show that as spacing gets smaller, stresses rise; the difference between the 1 μm and 4 μm pitch is roughly 30%. With this model, we can study the number of vias that we can safely put under a POA while still remaining within a safe level of ILD stress. And it was only with the COMSOL model that we could determine the areas of peak stress and understand how failures could arise. ■

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The STMicroelectronics COMSOL User Group

The popularity of the COMSOL Conferences conducted around the world each year attests to the benefit of being able to sit down with other COMSOL users to exchange tips and experiences. With this in mind, Lucia Zullino and Luca Cecchetto have formed an informal User Group inside STMicroelectronics with roughly 15 COMSOL users who meet at least once every quarter.

“The User Group meetings have been a valuable tool for me to discuss COMSOL products with my colleagues,” explains Sarah Burgarella, who has been a user since 2006. “Even though we are all working on different topics, we can still learn a great deal from each other. The User Group makes us all more efficient with the software.” She works at ST’s e-health group at the Agrate facility, which is working with COMSOL to simulate dielectrophoresis (DEP), a method for the manipulation and separation of biological cells under the action of high-gradient electric fields, which in turn can be used for lab-on-chip devices.

“These meetings are beneficial to us because we would like to use the software to examine a wide variety of things and especially for sensors,” adds Dario Paci of the Technology R&D department. “Although I had already used COMSOL during my studies at the University of Pisa, I still attend the User Group meetings to get even more knowledge about the package.”

The User Group is particularly useful for those who are somewhat new to the package, an example being a team of seven people from the MEMS group, located in Cornaredo. They are working with COMSOL on the design of accelerometers and gyroscopes, among other products. Their main use of COMSOL Multiphysics deals with coupled problems involving structural mechanics and electrostatics, but microfluidics and acoustics will also be studied. Notes Francesco Procopio, “Because we are new to COMSOL Multiphysics, the User Group meetings should be valuable for us to get input from our colleagues in Agrate, who have been using COMSOL for several years.”